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Kathy Manke Avago Technologies Limited 4380 Ziegler Road Fort Collins, CO 80525			EXAMINER VERBITSKY, GAIL KAPLAN	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/817,265  
Filing Date: April 02, 2004  
Appellant(s): FAOUR ET AL.

**MAILED**

DEC 12 2007

**GROUP 2800**

\_\_\_\_\_  
Robert Nelson  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 09/04/2007 appealing from the Office action mailed 07/20/2007, 04/05/2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

Davidson et al. (US 5639163 A)

Deng (U.S. 6911861)

Vergis (US 6453218 B1)

Audy et al. (US 5195827 A)

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3, 7-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5639163 A (Davidson, Evan Ezra et al., hereinafter DAVIDSON) in view of PRIOR ART by DENG (U.S. 6911861) [hereinafter Prior Art].

DAVIDSON discloses or suggests an integrated circuit as claimed by Applicant in Claims 1-3, 7-17 comprising:

Regarding Claim 1: DAVIDSON discloses an integrated circuit comprising a number of pads;

a constant current source (power supply, Fig. 2) to provide a current I1;

a thermal diode D1 that receives said current I1, said thermal diode being coupled between first C4A and second (ground pad, not explicitly shown) ones of said pads;

an analog to digital converter 36 to

i) receive a forward bias voltage (V1) of the thermal diode D1 (Col. 2, Lines 49-51), and

ii) output (to microprocessor 37, Col. 3, Lines 61-64) a digital representation of the forward bias voltage (V2 -V1).

Regarding Claim 7: DAVIDSON discloses an integrated circuit comprising a constant current source to provide first and second currents of different

magnitudes;

first D1 and second D2 thermal diodes that respectively receive said first I1 and second I2 currents;

a comparator 32 (Fig. 3) to receive forward bias voltages of each of the thermal diodes, to compare the forward bias voltages, and to output a voltage difference indicative of a temperature of the integrated circuit.

Further regarding Claims 2-3 and 17: DAVIDSON discloses logic 37 to receive the digital representation of the forward bias voltage and calculate a temperature of the integrated circuit (Col. 3, Lines 50-52; and Col. 4, Lines 1-4), wherein said logic comprises a temperature look-up table 39 as claimed by Applicant in Claims 3 and 17.

Further regarding Claims 1, 7: DAVIDSON discloses a third one of said pads is provided to receive a reference current, said third pad C4B being coupled to an input of said constant current source as claimed by Applicant. Davidson does not explicitly teach a reference current circuit coupled to the third pad.

Further regarding Claims 8-10 and 16: DAVIDSON discloses the thermal diodes are positioned adjacent one another (Col. 2, Lines 45-49) as claimed by Applicant in Claim 8, and the first and second currents have a known relationship as claimed by Applicant in Claims 9 and 16, and further regarding Claim 10, the second current I2 is an integer multiple of the first current I1 (Col. 3, Lines 6-15; e.g., a ratio of 100:1).

Further regarding Claim 11: DAVIDSON discloses the comparator 32 is a differential amplifier.

Further regarding Claims 12 and 14: DAVIDSON discloses the integrated circuit

further comprising an analog to digital converter 36 to

- i) receive the voltage difference output by the differential amplifier, and
- ii) output a digital representation of the voltage difference.

Further regarding Claims 13 and 15: DAVIDSON discloses the integrated circuit

further comprising logic 37 to receive the digital representation of the voltage difference and calculate a temperature of the integrated circuit.

DAVIDSON, to summarize, discloses or suggests all the limitations as claimed by Applicant in Claims 1-3, 7-17, as described above, except DAVIDSON'S power supply  $V_p$  is off the "chip area" as indicated by chip 12 (Fig. 12), therefore is not considered to be a pad of the integrated circuit disclosed by DAVIDSON. DAVIDSON as described above, Davidson does not explicitly teach a reference current circuit coupled to the third pad, and that the said reference current thereby serving to control the constant current source.

Prior Art discloses in Fig. 1 a device in the field of applicant's endeavor comprising a current generating circuit 104 generating a current proportional to a reference current being regulated (controlled/ adjusted) by a resistor (variable current reference, thus, adjusting the constant current source to a device of interest) coupled to the circuit by means of a (third) pad 108.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device, disclosed by Davidson, so as to add a reference current by means of a third pad to a current source, disclosed by Prior Art, in order to generate a current proportional to a temperature, as taught by Prior Art, so as to obtain more accurate results by varying current proportionally to temperature change in the IC, as very well known in the art.

Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over DAVIDSON and PRIOR ART as applied to claims 1-3, 7-17 above, and further in view of US 6453218 B1 (Vergis, George, hereinafter VERGIS).

DAVIDSON and PRIOR ART, to summarize, disclose or suggest all the limitations as claimed by Applicant in Claims 4 and 19, as described above in Paragraph 9 as applied to Claims 1-3, 7-17 and 20 further including the limitations that the microprocessor 37 has an input that receives the digital representation of the differential input voltage, the digital representation of the voltage difference (between the two forward bias voltages) as claimed by Applicant, and includes a look-up table for converting those values to temperature values, and the microprocessor 37 outputs these values over a suitable bus 41. DAVIDSON discloses that the microprocessor 37 may compare the measured value to a limit and provide an over-temperature output signal to a lead 40 (Col. 3, Line 61 - Col. 4, Line 8).

They as described above, do not explicitly disclose a register to store the digital representation of the forward bias voltage, the digital representation of the voltage difference as claimed by Applicant, said register being readable during normal operation of the integrated circuit as claimed by Applicant.

VERGIS discloses it is known in the art to store the digital representation of a temperature that is based on the forward bias voltage across a diode in a register area 104 (Col. 3, Lines 15-33). VERGIS further discloses that it is advantageous to store the digital representation of temperature in a register in order to benefit from the ability to periodically store the data as it is measured, but only read it at convenient times that will

not interfere with other processor operations (Col. 3, Lines 34-54).

VERGIS is evidence that ordinary workers in the field of temperature measurement in integrated circuits would recognize the benefit of adding a register being readable during normal operation of the integrated circuit as taught by VERGIS for the device of DAVIDSON and Prior ART in order to benefit from not interfering with other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a register being readable during normal operation for the transmitted output signal of DAVIDSON and PRIOR ART in order to not interfering with other processor operations by allowing the microprocessor to choose when the temperature data will be transmitted as taught by VERGIS.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over DAVIDSON and PRIOR ART as applied to claims 1-3, 7-17 above and further in view of US 5195827 A (AUDY; Jonathan M. et al., hereinafter AUDY).

DAVIDSON and PRIOR ART, to summarize, disclose or suggest all the limitations as claimed by Applicant in Claim 18, as described above, as applied to Claims 1-3, 7-17 and 20 further including the limitations of one analog to digital converter 36 receiving the output of comparator 32. DAVIDSON further disclosed that the currents should be precisely controlled by selecting external resistors with precisely known values.



They as described above, do not explicitly disclose one or more analog to digital converters receiving the first and second currents and outputting digital representations of said currents to logic.

AUDY discloses an ammeter 24 and analog to digital converter 38 for providing the current data to the central processor 36.

AUDY is evidence that ordinary workers in the field of semiconductor device temperature sensing would recognize the benefit of using an analog to digital converter as taught by AUDY for the precisely known resistors of DAVIDSON and PRIOR ART in order to measure the currents for better accuracy without requiring the resistors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute an analog to digital converter for the precise resistors controlling the current of DAVIDSON and PRIOR ART in order to use multiple excitations and cancel parasitic base and emitter resistances, as taught by AUDY.

#### **(10) Response to Argument**

Applicant's arguments filed in the Appeal Brief have been fully considered. Applicant questions the Office Action statement that "the prior art discloses variable current reference, which is used to adjust the constant current source". Applicant states that the prior art outputs current based on "the voltage and not an input current received on a third pad as claimed" (page 7 of appeal brief) (1). This argument is not persuasive because this limitation has not been claimed in claims 1 and 7. It is the claims that

define the claimed invention, and it is claims, not specification that are anticipated or unpatentable. Constant v. Advanced Micro-Devices, Inc., 7 USPQ2d 1064.

What is claimed by applicant is "the third pad is provided to receive a reference current, said third pad being coupled to an input of said constant current source, said reference current serving to control the constant current source" (2). These two statements, (1) and (2), are not quite the same. Applicant does not claim that the constant current is (and not some voltage) is a source for the reference current.

Deng discloses a reference current source, this reference current source is, inherently, configured to control / adjust any current source which the reference current source of Deng is coupled to. This would imply, that if the reference current source is coupled to the constant current source of Davidson, it would control/ adjust it. The fact that the source for reference current source of Deng is voltage is irrelevant because applicant has never claimed that the source for the reference current is a current source or particularly, a constant current. In addition, the circuit of Deng generates output current which may be used as biasing reference current (col. 2, lines 30-37). This biasing reference current would be coupled to the third pad in order to adjust the constant current of Davidson (as very well known in the art) since the current of Davidson is also coupled to the pad.

Applicant states that Davidson cannot be combined with Deng. This argument is not persuasive because:

A) the Examiner recognizes that there should be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). The references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

B) Davidson discloses all the subject matter as claimed by applicant with the exception of means for regulating a constant current. Deng discloses a device in the field of applicant's endeavor comprising means for regulating the constant current by means of a pad/ contact/ electrical connection.

C) It is very well known in the art that any current needs and can be regulated depending on a circuit it supplies.

Applicant questions how the circuit of Davidson will operate in combination with the constant current regulator of Deng to come to the claimed invention. In response to this

please note, A) the references are from the same field of endeavor as the applicant's invention, B) neither Davidson or Deng teach anything in their disclosures that would suggest that the two are not combinable. C) Davidson does not rule out having a constant current regulator. If, for example, Davidson teaches some specific current value that is out of limit of capability of the constant current regulator of Deng, then the Examiner would agree with the arguments. However, neither references, nor the Applicant disclose specific operation values of the circuits that could question a success of the combination by the Examiner.

The Examiner's position is that the Examiner provided the Applicant with the combination of the references clearly showing the reference current circuit coupled to the constant current circuit to control it and to provide the reference current, as very well known in the art of measuring temperature in IC whose output signal can be temperature dependent and thus, inaccurate.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

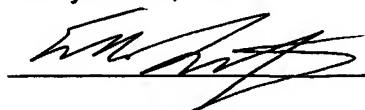


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